

EXHIBIT 036

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)


“Integrated circuit with data communication network and IC design method”

'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip ¹
1. An integrated circuit comprising:	<p>Without conceding that the preamble of claim 1 of the '2893 Patent is limiting, the Motorola Edge+ Gen 2 (hereinafter, the “Motorola product”) includes an integrated circuit.</p> <p>For example, the Motorola product includes the Qualcomm Snapdragon 8 Gen 1 Mobile Platform system on chip (hereinafter, the “Snapdragon SoC”).</p> <div data-bbox="491 574 940 1062">  </div> <div data-bbox="1102 565 1696 623"> <h2>Motorola Edge+ Gen 2</h2> </div> <div data-bbox="1102 646 1667 672"> <p>Featuring a Snapdragon 8 Gen 1 Mobile Platform</p> </div> <div data-bbox="1102 699 1827 987"> <p>The Motorola edge+ was born for 5G speed. This state-of-the-art smartphone gives you up to 2 full days of power, lightning-fast speed, and pro-quality features for doing more of what you love. Leave lag time behind with a massive 256 GB+ memory and blazing-fast premium Snapdragon mobile platform. Enjoy days of entertainment on a beautiful display that wraps around the edges and has superior stereo-quality sound. Get the best of Android OS without the extra baggage.</p> </div> <div data-bbox="1142 1089 1247 1110"> <p>Learn more</p> </div> <div data-bbox="464 1175 1610 1213"> <p>https://www.qualcomm.com/snapdragon/device-finder/motorola-edge--gen-2</p> </div>

¹ The Motorola product is charted as a representative product made used, sold, offered for sale, and/or imported by Motorola. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

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a plurality of functional blocks; and	<p>The Snapdragon SoC included in the Motorola product includes a plurality of functional blocks, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU):</p> <div data-bbox="472 443 865 574">  <p>Snapdragon 8 mobile platform Gen 1</p> </div> <div data-bbox="1434 467 1713 488">SPECIFICATIONS & FEATURES</div> <div data-bbox="472 641 680 662"> Artificial Intelligence <hr/> <p>Qualcomm® Adreno™ GPU</p> <hr/> <p>Qualcomm® Kryo™ CPU</p> <hr/> <p>Qualcomm® Hexagon™ Processor</p> <ul style="list-style-type: none"> • Fused AI Accelerator <ul style="list-style-type: none"> • Hexagon Tensor Accelerator • Hexagon Vector eXtensions • Hexagon Scalar Accelerator • Support for mix precision (INT8+INT16) • Support for all precisions (INT8, INT16, FP16) <hr/> <p>Qualcomm® Sensing Hub</p> <hr/> <p>5G Modem-RF System</p> <hr/> <p>Snapdragon X65 5G Modem-RF System</p> <ul style="list-style-type: none"> • 5G mmWave and sub-6 GHz, standalone (SA) and non-standalone (NSA) modes, FDD, TDD • Dynamic Spectrum Sharing • mmWave: 1000 MHz bandwidth, 8 carriers, 2x2 MIMO • Sub-6 GHz: 300 MHz bandwidth, 4x4 MIMO • Qualcomm® 5G PowerSave 2.0 • Qualcomm® Smart Transmit™ 2.0 technology • Qualcomm® Wideband Envelope Tracking • Qualcomm® AI-Enhanced Signal Boost • Global 5G multi-SIM <hr/> <p>Downlink: Up to 10 Gbps</p> <hr/> <p>Multimode support: 5G NR, LTE including CBRS, WCDMA, HSPA, TD-SCDMA, CDMA 1x, EV-DO, GSM/EDGE</p> <hr/> <p>Camera</p> <hr/> <p>Qualcomm Spectra™ Image Signal Processor</p> <ul style="list-style-type: none"> • Triple 18-bit ISPs • Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP) • Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag • Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag • Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag • Up to 200 Megapixel Photo Capture <hr/> <p>Rec. 2020 color gamut photo and video capture</p> <hr/> <p>Up to 10-bit color depth photo and video capture</p> <hr/> <p>8K HDR Video Capture + 64 MP Photo Capture</p> <hr/> <p>10-bit HEIF: HEIC photo capture, HEVC video capture</p> <hr/> <p>Video Capture Formats: HDR10+, HDR10, HLG, Dolby Vision</p> <hr/> <p>8K HDR Video Capture @ 30 FPS</p> <hr/> <p>4K Video Capture @ 120 FPS</p> <hr/> <p>Slow-mo video capture at 720p @ 960 FPS</p> <hr/> <p>Bokeh Engine for Video Capture</p> <hr/> <p>Video super resolution</p> <hr/> <p>Multi-frame Noise Reduction (MFNR)</p> <hr/> <p>Locally Motion Compensated Temporal Filtering</p> <hr/> <p>Multi-Frame and triple exposure staggered/digital overlap HDR dual-sensor support</p> <hr/> <p>AI-based face detection, auto-focus, and auto-exposure</p> <hr/> <p>CPU</p> <hr/> <p>Kryo CPU</p> <ul style="list-style-type: none"> • Up to 3.0 GHz*, with Arm Cortex-X2 technology • 64-bit Architecture <hr/> <p>Visual Subsystem</p> <hr/> <p>Adreno GPU</p> <ul style="list-style-type: none"> • Vulkan® 1.1 API support • HDR gaming (10-bit color depth, Rec. 2020 color gamut) • Physically Based Rendering • Volumetric Rendering • Adreno Frame Motion Engine • API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1 • Hardware-accelerated H.265 and VP9 decoder • HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision <hr/> <p>Security</p> <hr/> <p>Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU)</p> <hr/> <p>Trust Management Engine</p> <hr/> <p>Qualcomm® wireless edge services (WES) and premium security features</p> <hr/> <p>Qualcomm® 3D Sonic Sensor and Qualcomm 3D Sonic Max (fingerprint sensor)</p> <hr/> <p>Qualcomm® Type-1 Hypervisor</p> </div>

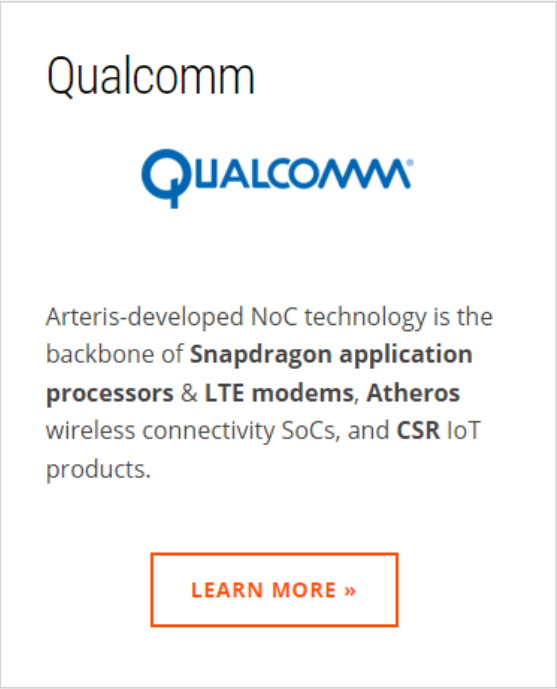
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	<div data-bbox="472 316 667 337"> Wi-Fi & Bluetooth* </div> <div data-bbox="472 354 871 836"> <p>Qualcomm® FastConnect™ 6900 System</p> <ul style="list-style-type: none"> • Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax), Wi-Fi 5 (802.11ac), 802.11a/b/g/n • Wi-Fi Spectral Bands: 24 GHz, 5 GHz, 6 GHz • Peak speed: 3.6 Gbps • Channel Bandwidth: 20/40/80/160 MHz • 8-stream sounding (for 8x8 MU-MIMO) • MIMO Configuration: 2x2 (2-stream) • MU-MIMO (Uplink & Downlink) • 4K QAM • OFDMA (Uplink & Downlink) • Dual-band simultaneous (2x2 + 2x2) • Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal <p>Integrated Bluetooth</p> <ul style="list-style-type: none"> • Bluetooth Features: Bluetooth 5.2, LE Audio, Dual Bluetooth antennas • Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm® aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio </div> <div data-bbox="472 873 653 894"> snapdragon.com </div> <div data-bbox="472 966 1711 1071"> <p><small>* Exact speed measured at 2.995 GHz Certain optional features available subject to Carrier and OEM selection for an additional fee. Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm SGI PowerSave, Qualcomm Kryo, Qualcomm Smart Transmit, Qualcomm Wideband Envelope, Qualcomm AI-Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Aqstic, Qualcomm 3D Sonic Sensor, Qualcomm Type-Hypervisor, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries. Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kryo, Smart Transmit, Qualcomm Spectra, Qualcomm Aqstic, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd. ©2021 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.</small></p> </div> <div data-bbox="472 1133 1522 1203"> https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/snapdragon-8-gen-1-mobile-platform-product-brief.pdf </div> <div data-bbox="924 316 982 337"> Audio </div> <div data-bbox="924 354 1323 500"> <p>Qualcomm Aqstic™ audio codec (WCD9385)</p> <p>New Qualcomm Aqstic smart speaker amplifier (WSA8835)</p> <p>Total Harmonic Distortion + Noise (THD+N), Playback: -108dB</p> <p>Qualcomm Audio and Voice Communication Suite</p> </div> <div data-bbox="924 532 1001 553"> Display </div> <div data-bbox="924 570 1302 776"> <p>On-Device Display Support:</p> <ul style="list-style-type: none"> • 4K @ 60 Hz • QHD+ @ 144 Hz <p>Maximum External Display Support: up to 4K @ 60 Hz</p> <ul style="list-style-type: none"> • 10-bit color depth, Rec. 2020 color gamut • HDR10 and HDR10+ <p>Demura and subpixel rendering for OLED Uniformity</p> </div> <div data-bbox="1369 289 1465 310"> Charging </div> <div data-bbox="1369 326 1669 347"> <p>Qualcomm® Quick Charge™ 5 Technology</p> </div> <div data-bbox="1369 375 1461 396"> Location </div> <div data-bbox="1369 412 1705 578"> <p>GPS, Glonass, BeiDou, Galileo, QZSS, NavIC capable</p> <p>Dual Frequency GNSS (L1/L5)</p> <p>Sensor-Assisted Positioning</p> <ul style="list-style-type: none"> • Urban pedestrian navigation with sidewalk accuracy • Global freeway lane-level vehicle navigation </div> <div data-bbox="1369 613 1455 634"> Memory </div> <div data-bbox="1369 651 1711 698"> <p>Support for LP-DDR5 memory up to 3200 MHz</p> <p>Memory Density: up to 16 GB</p> </div> <div data-bbox="1369 727 1602 748"> General Specifications </div> <div data-bbox="1369 764 1717 870"> <p>Full Suite of Snapdragon Elite Gaming™ features</p> <p>4 nm Process Technology</p> <p>USB Version 3.1; USB Type-C Support</p> <p>Part Number: SM8450</p> </div>
a data communication network comprising a plurality of	The Snapdragon SoC included in the Motorola product includes a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, either literally or under the doctrine of equivalents.

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<p>network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,</p>	<p>The Snapdragon SoC included in the Motorola product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) as a data communication network:</p> <div data-bbox="478 451 1031 1136">  <p>Qualcomm</p> <p>Arteris-developed NoC technology is the backbone of Snapdragon application processors & LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products.</p> <p>LEARN MORE »</p> </div> <p>https://web.archive.org/web/20210514110614/https://www.artemis.com/customers</p>

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	<p data-bbox="541 293 1325 337">Certain Arteris Technology Assets Acquired</p> <p data-bbox="747 370 1115 394">by Kurt Shuler, on October 31, 2013</p> <p data-bbox="478 435 1220 459">Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP</p> <p data-bbox="478 487 1381 589">SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. (“Qualcomm”), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris.</p> <p data-bbox="478 626 1325 768">“Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris’ Network-on-Chip interconnect IP technology.</p> <p data-bbox="1199 813 1346 837">ARTERIS IP</p> <p data-bbox="1083 889 1346 906"><i>K. Charles Janac, President and CEO, Arteris</i></p> <p data-bbox="464 971 1766 1044">https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team</p> <p data-bbox="464 1092 1843 1157">A large SoC, such as the Snapdragon SoC included in the Motorola product may include multiple classes of Arteris NoC data communication network:</p>

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	<h2 data-bbox="499 300 1543 349">Logical Interconnect Topology Development</h2> <p data-bbox="499 365 1365 389">FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</p> <ul data-bbox="499 852 1711 950" style="list-style-type: none"> • ArChip16 Example: Large SoCs have multiple classes of interconnect <ul style="list-style-type: none"> – Non-coherent, Coherent, Control/Status, Observability, etc. • Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility <p data-bbox="472 990 1827 1023"> ARTERIS IP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 9 </p> <p data-bbox="462 1079 1848 1153">See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.</p> <p data-bbox="462 1193 1869 1307">The Arteris NoC in the Snapdragon SoC included in the Motorola product is a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks.</p>

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	<p>For example, the Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

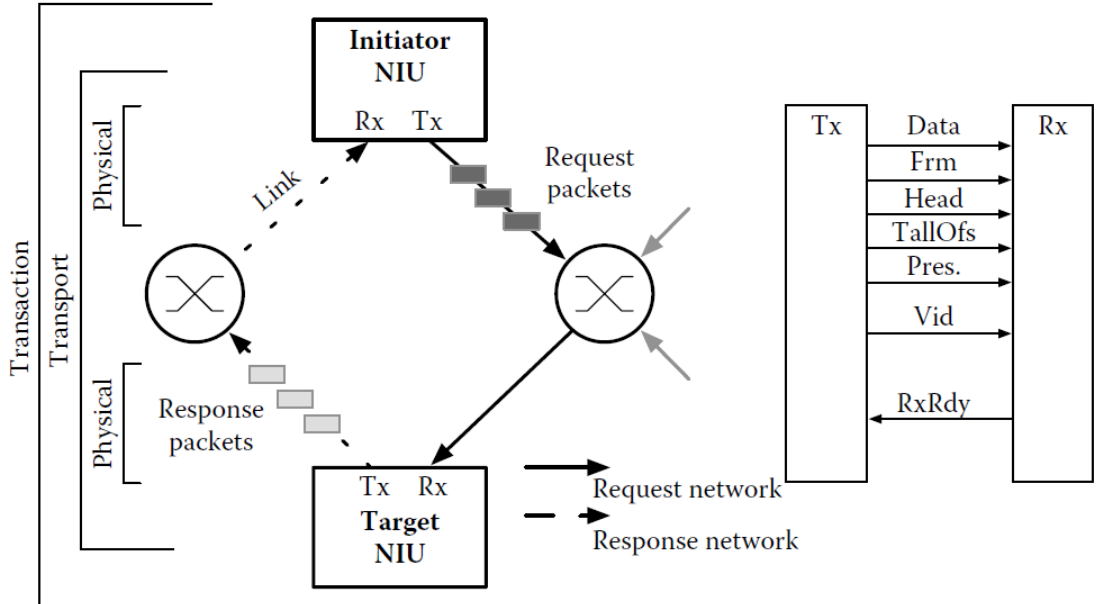
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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”).</p> <p>As a further illustration, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312.</p>

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each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,	<p>In the Arteris NoC utilized by the Snapdragon SoC included in the Motorola product, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, either literally or under the doctrine of equivalents.</p> <p>For example, the “Arteris NTTP protocol is packet-based” and the packets, which have “header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address,” are “transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes”:</p> <p>11.3.1.2 Transport Layer</p> <p>The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313.</p> <p>As yet a further illustration, packets in the Arteris NoC are “delivered as words that are sent along links and “[o]ne link (represented in Figure 11.1) defines the following signals”:</p>

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maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in [Figure 11.1](#)) defines the following signals:

- **Data**—Data word of the width specified at design-time.
- **Frm**—When asserted high, indicates that a packet is being transmitted.
- **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only.
- **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only.
- **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in [Figure 11.2](#)).
- **Vld**—Data valid: when asserted high, indicates that a word is being transmitted.
- **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy.

This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

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	<p><i>Id.</i> at 313-314.</p> <p>As a further example, the packets sent in the Arteris NoC are “composed of cells that are organized into fields, with each field carrying specific information”:</p> <table><tr><th>Field</th><th>Size</th><th>Function</th></tr><tr><td>Opcode</td><td>4 bits/3 bits</td><td>Packet type: 4 bits for requests, 3 bits for responses</td></tr><tr><td>MstAddr</td><td>User Defined</td><td>Master address</td></tr><tr><td>SlvAddr</td><td>User Defined</td><td>Slave address</td></tr><tr><td>SlvOfs</td><td>User Defined</td><td>Slave offset</td></tr><tr><td>Len</td><td>User Defined</td><td>Payload length</td></tr><tr><td>Tag</td><td>User Defined</td><td>Tag</td></tr><tr><td>Prs</td><td>User defined (0 to 2)</td><td>Pressure</td></tr><tr><td>BE</td><td>0 or 4 bits</td><td>Byte enables</td></tr><tr><td>CE</td><td>1 bit</td><td>Cell error</td></tr><tr><td>Data</td><td>32 bits</td><td>Packet payload</td></tr><tr><td>Info</td><td>User Defined</td><td>Information about services supported by the NoC</td></tr><tr><td>Err</td><td>1 bit</td><td>Error bit</td></tr></table>	Field	Size	Function	Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses	MstAddr	User Defined	Master address	SlvAddr	User Defined	Slave address	SlvOfs	User Defined	Slave offset	Len	User Defined	Payload length	Tag	User Defined	Tag	Prs	User defined (0 to 2)	Pressure	BE	0 or 4 bits	Byte enables	CE	1 bit	Cell error	Data	32 bits	Packet payload	Info	User Defined	Information about services supported by the NoC	Err	1 bit	Error bit
Field	Size	Function																																						
Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses																																						
MstAddr	User Defined	Master address																																						
SlvAddr	User Defined	Slave address																																						
SlvOfs	User Defined	Slave offset																																						
Len	User Defined	Payload length																																						
Tag	User Defined	Tag																																						
Prs	User defined (0 to 2)	Pressure																																						
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	StartOfs	2 bits	Start offset
	StopOfs	2 bits	Stop offset
	WrpSize	4 bits	Wrap size
	Rsv	Variable	Reserved
	CtlId	4 bits/3 bits	Control identifier, for control packets only
	CtlInfo	Variable	Control information, for control packets only
	EvtId	User defined	Event identifier, for event packets only

352928252415145430

Header

InfoLenMaster AddressSlave AddressPrsOpcode

Necker

TagErrSlave offsetStartOfsStopOfs

Data

BEData ByteBEData ByteBEData ByteBEData Byte

Data

BEData ByteBEData ByteBEData ByteBEData Byte

3231302726201914135430

Header

RsvLenInfoTagMaster AddressPrsOpcode

Data

CEData

Data

CEData

FIGURE 11.2
NTTP packet structure.

Networks-On-Chips Theory and Practice, <https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0>, at 313, 314-315.

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the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface,	<p>In the Arteris NoC utilized by the Snapdragon SoC included in the Motorola product, the plurality of network stations comprise a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”:</p> <p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

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	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>As a further illustration, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

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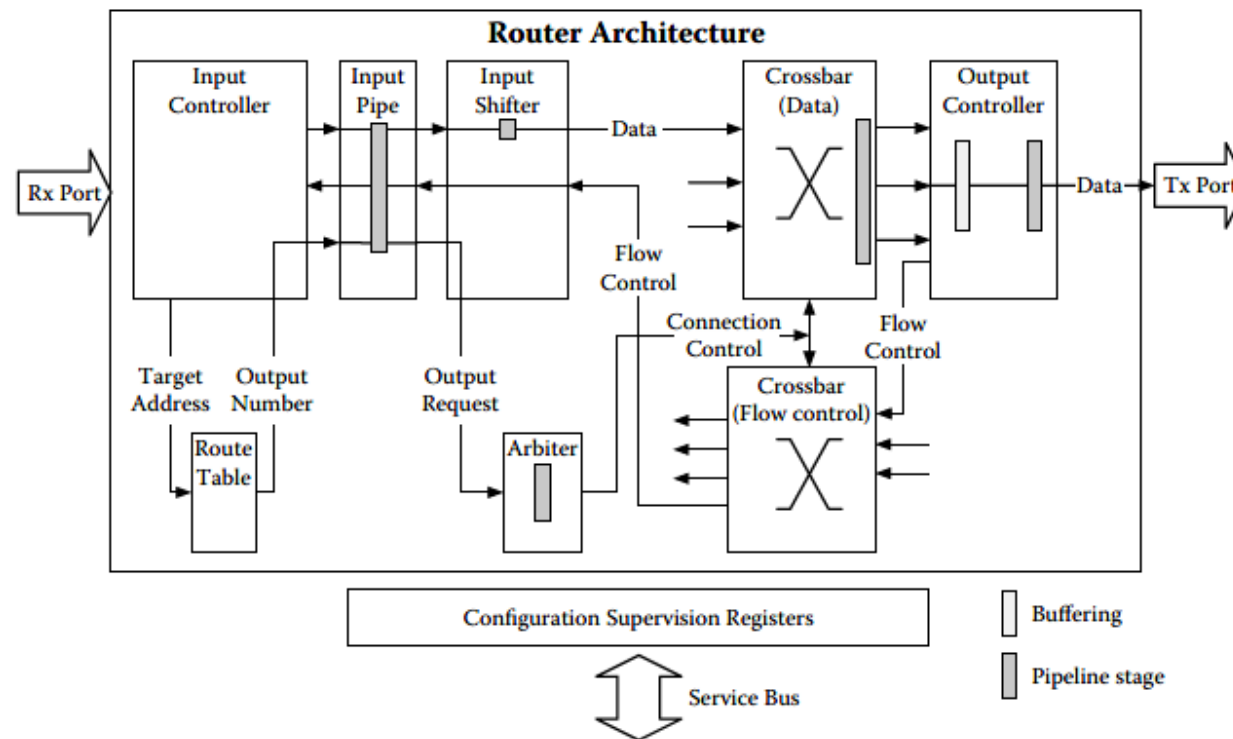
<p>'2893 Patent Claim</p>	<p>Motorola Product Including Snapdragon System on Chip¹</p>
	<p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312.</p> <p>As a further illustration of the routers in the Arteris NoC:</p>

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11.3.3.2 Routing

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address

**FIGURE 11.6**

Packet transportation unit: Router architecture.

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	<p>As a further illustration of the network interfaces in the Arteris NoC:</p> <p>11.3.2.1 Initiator NIU Units</p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.</p>

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	<p>11.3.2.2 Target NIU Units</p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always</p> <p><i>Id.</i> at 318.</p>
the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication	<p>In the Arteris NoC utilized in the Snapdragon SoC included in the Motorola product, the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further comprising M*N data storage elements, M being a positive integer, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”:</p>

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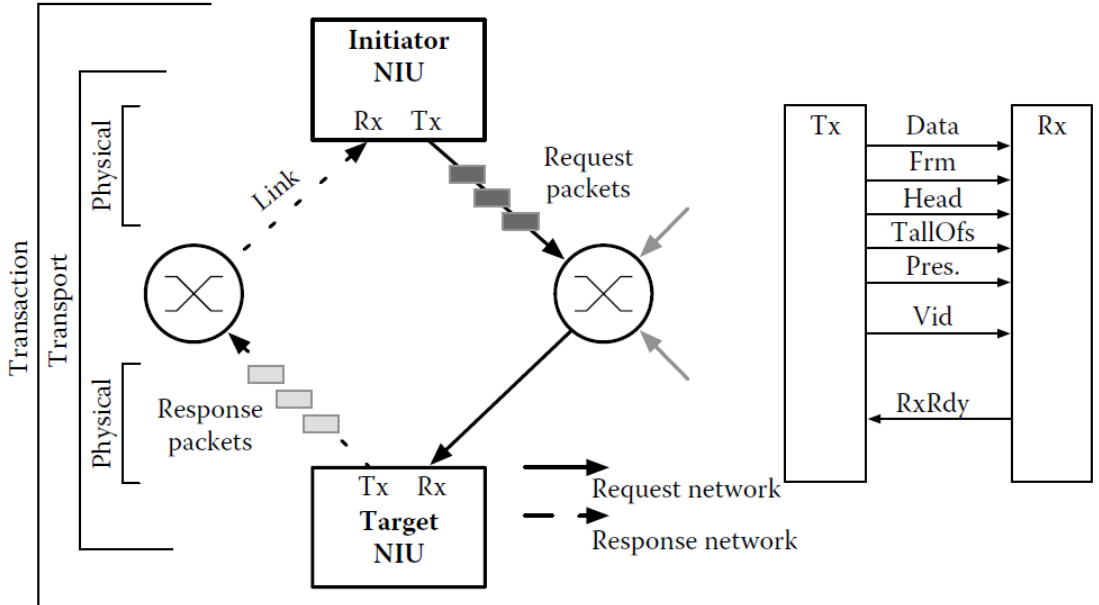
“Integrated circuit with data communication network and IC design method”

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network further comprising M*N data storage elements, M being a positive integer,	<p>11.3.1.1 Transaction Layer</p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> • A master sends request packets. • Then, the slave returns response packets. <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

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	<p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.</p> <p>As a further illustration, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”</p>

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	 <p>FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312.</p> <p>As a further example, a “delay pipeline is automatically inserted in the input controller to keep data and routing information in phase” and an input pipe “introduces a one-word-deep FIFO”:</p>

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	<p>Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the</p> <p>* * *</p> <p>The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 322.</p> <p>As a further example, the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element “with as many words as there are date pipelined in the crossbar”:</p>

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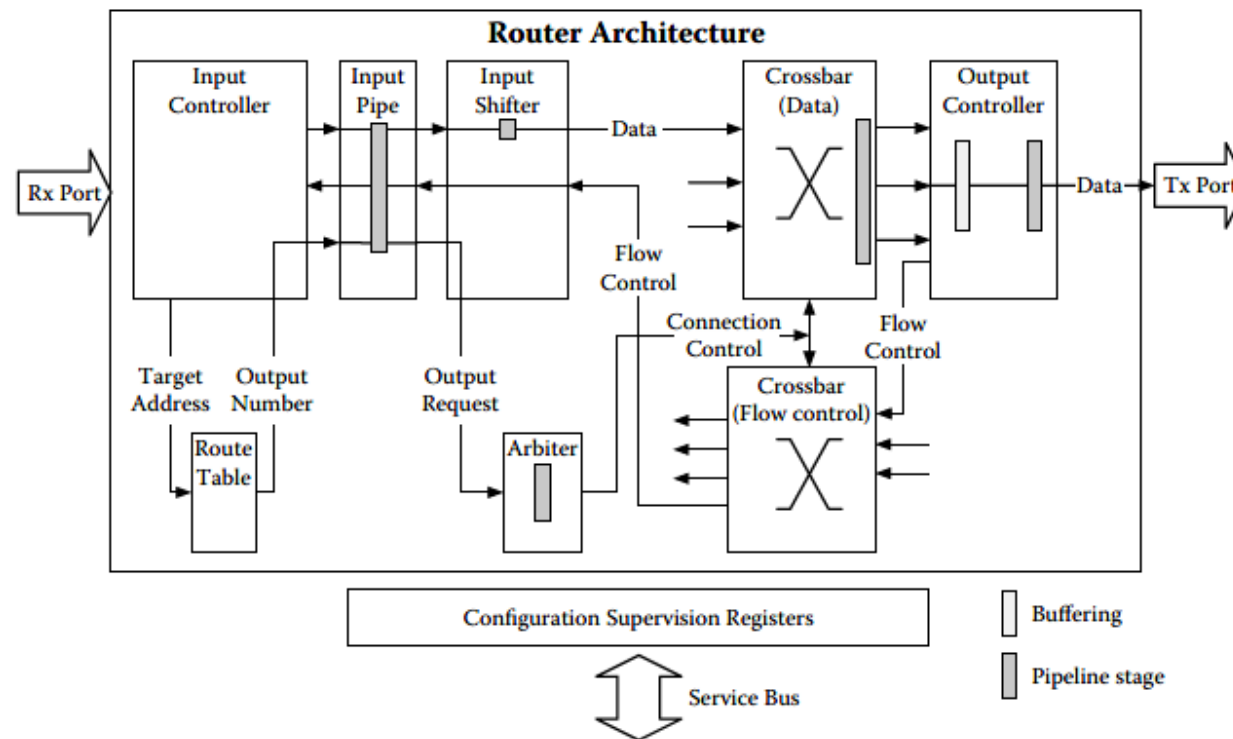
'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip ¹
	<p>The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of m muxes (one per output port), each having n inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as $\max(n, m)$.</p> <p>The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller.</p> <p><i>Id.</i> at 323.</p> <p>The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:</p>

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11.3.3.2 Routing

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address

**FIGURE 11.6**

Packet transportation unit: Router architecture.

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	<p><i>Id.</i> at 320.</p> <p>As another example, the “fwdPipe” parameter “introduces a true pipeline register on the forward signals” and “inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path”:</p> <p>get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path.</p> <p><i>Id.</i> at 323-324.</p>
the data communication introducing a delay of M*N cycles on the first communication channel when the data communication	<p>In the Arteris NoC utilized in the Snapdragon SoC included in the Motorola product, the data communication introducing a delay of M*N cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold, either literally or under the doctrine of equivalents.</p> <p>For example, a “delay pipeline is automatically inserted in the input controller to keep data and routing information in phase” and an input pipe “introduces a one-word-deep FIFO”:</p>

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<p>network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.</p>	<p>Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the</p> <p>* * *</p> <p>The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle.</p> <p>See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 322.</p> <p>As a further example, the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element “with as many words as there are date pipelined in the crossbar”:</p>

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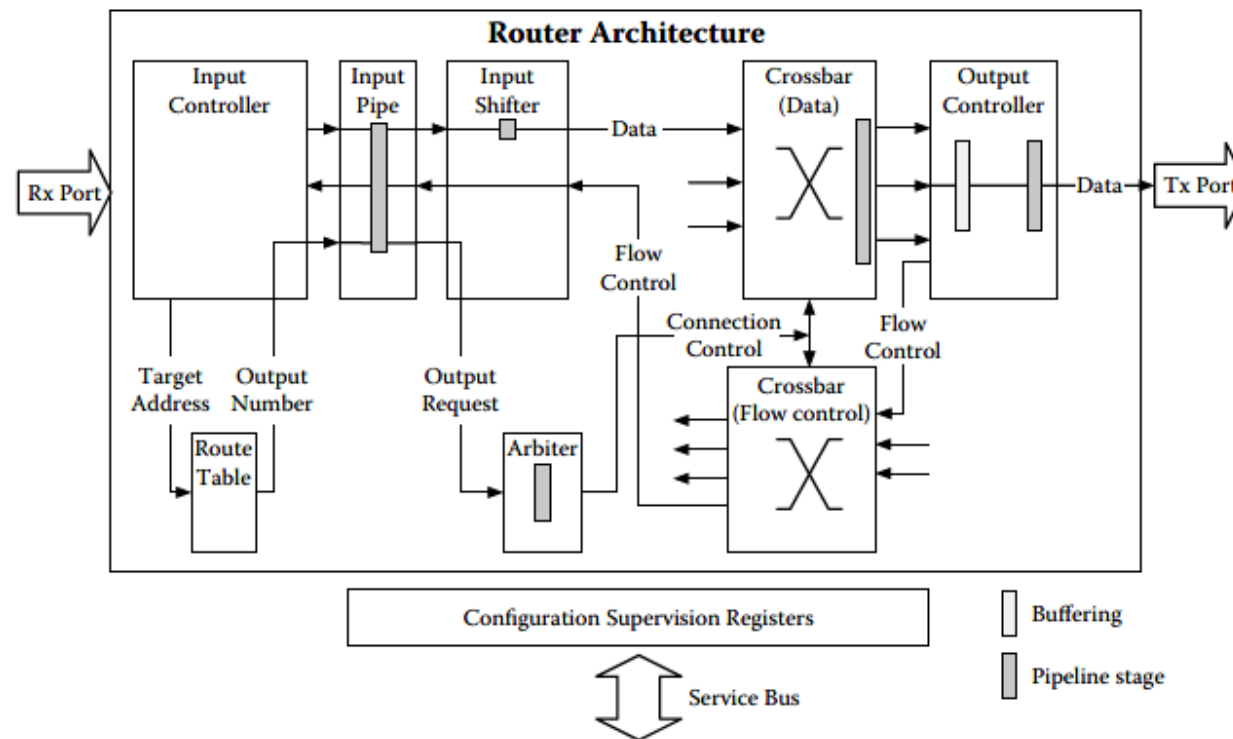
'2893 Patent Claim	Motorola Product Including Snapdragon System on Chip ¹
	<p>The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of m muxes (one per output port), each having n inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as $\max(n, m)$.</p> <p>The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller.</p> <p><i>Id.</i> at 323.</p> <p>The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:</p>

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	<p><i>Id.</i> at 320.</p> <p>As another example, the “fwdPipe” parameter “introduces a true pipeline register on the forward signals” and “inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path”:</p> <p>get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path.</p> <p><i>Id.</i> at 323-324.</p> <p>As another example, pipelines may be automatically inserted by the Arteris NoC to close timing:</p>


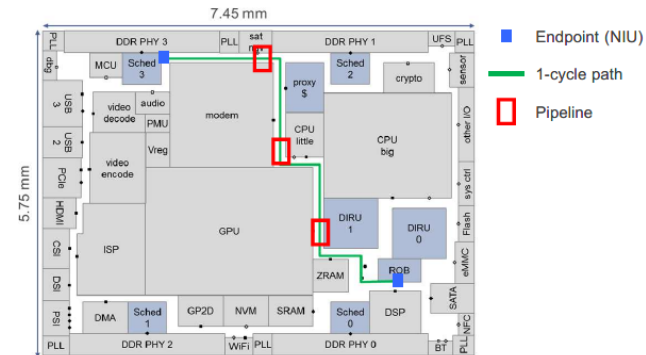
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	<div data-bbox="499 305 1371 959"> <h3 data-bbox="541 365 1119 407">Adding Pipelines Automatically</h3> <ul data-bbox="541 505 905 678" style="list-style-type: none"> ○ Evaluate all timing arcs in the NoC interconnect ○ Distance and logic depth dictate number of pipeline stages ○ Placement of the NoC units is predicted by FlexNoC <p data-bbox="541 760 877 808">  = New pipelines inserted by FlexNoC Physical to close timing </p> </div> <p data-bbox="464 982 1472 1057"> Using SoC Interconnect IPs to Improve Physical Layout, http://mpsoc-forum.org/archive/2015/slides/45B-Charles%20Janac.pdf, at slide 14. </p> <p data-bbox="464 1105 1854 1216"> As a further illustration, the Arteris NoC includes pipelining for distance spanning when traveling “~6mm” has a propagation delay of “~400ps/mm”, requiring at least “2400ps to span the Distance”; thus requiring “at least 3 pipeline stages and 4 clock cycles to meet timing.” </p>

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	<div data-bbox="525 305 1722 365"> <h2 style="color: orange;">Wire Delays – Can't Cross a Chip in 1 Clock Cycle</h2> </div> <div data-bbox="525 370 1407 402"> <p>PHYSICAL DISTANCE DICTATES THE NUMBER OF PIPELINE STAGES</p> </div> <div data-bbox="678 443 879 680">  <p style="text-align: center;">Clock Cycles</p> </div> <div data-bbox="525 745 1518 885"> <ul style="list-style-type: none"> • Interconnect Frequency: 1.2GHz = 833ps • Distance to travel = ~6mm • Propagation delay = ~400ps/mm in 16nm FinFET; Needs 2400ps to span the distance • Requires at least 3 pipeline stages and 4 clock cycles to meet timing </div> <div data-bbox="537 898 1797 963" style="background-color: orange; padding: 5px;"> <p>Large 14nm FinFET SoC may have >6,000 pipelines with 6K factorial pipeline combinations and 60 timing parameters – Too much for human comprehension!</p> </div> <div data-bbox="1178 427 1820 779">  <p>7.45 mm</p> <p>5.75 mm</p> <p>■ Endpoint (NIU)</p> <p>— 1-cycle path</p> <p>□ Pipeline</p> </div> <div data-bbox="495 990 634 1019"> <p>ARTERIS^{IP}</p> </div> <div data-bbox="1083 995 1243 1016"> <p>ISPD 2018, 28 March 2018</p> </div> <div data-bbox="1617 995 1837 1016"> <p>Copyright © 2018 Arteris IP 3</p> </div> <div data-bbox="453 1047 1854 1123"> <p>See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 3.</p> </div>